**Bug-1 Report**

**Group-5**

1. **Failing Test name**

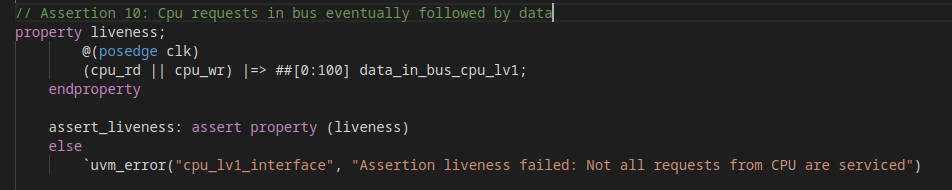
Data cache read Miss Test

1. **Test description (Describe the planned scenario and the expected result)**

read\_miss\_dcache: A basic read on the data cache was executed, and was expected to get data from level-2 cache.

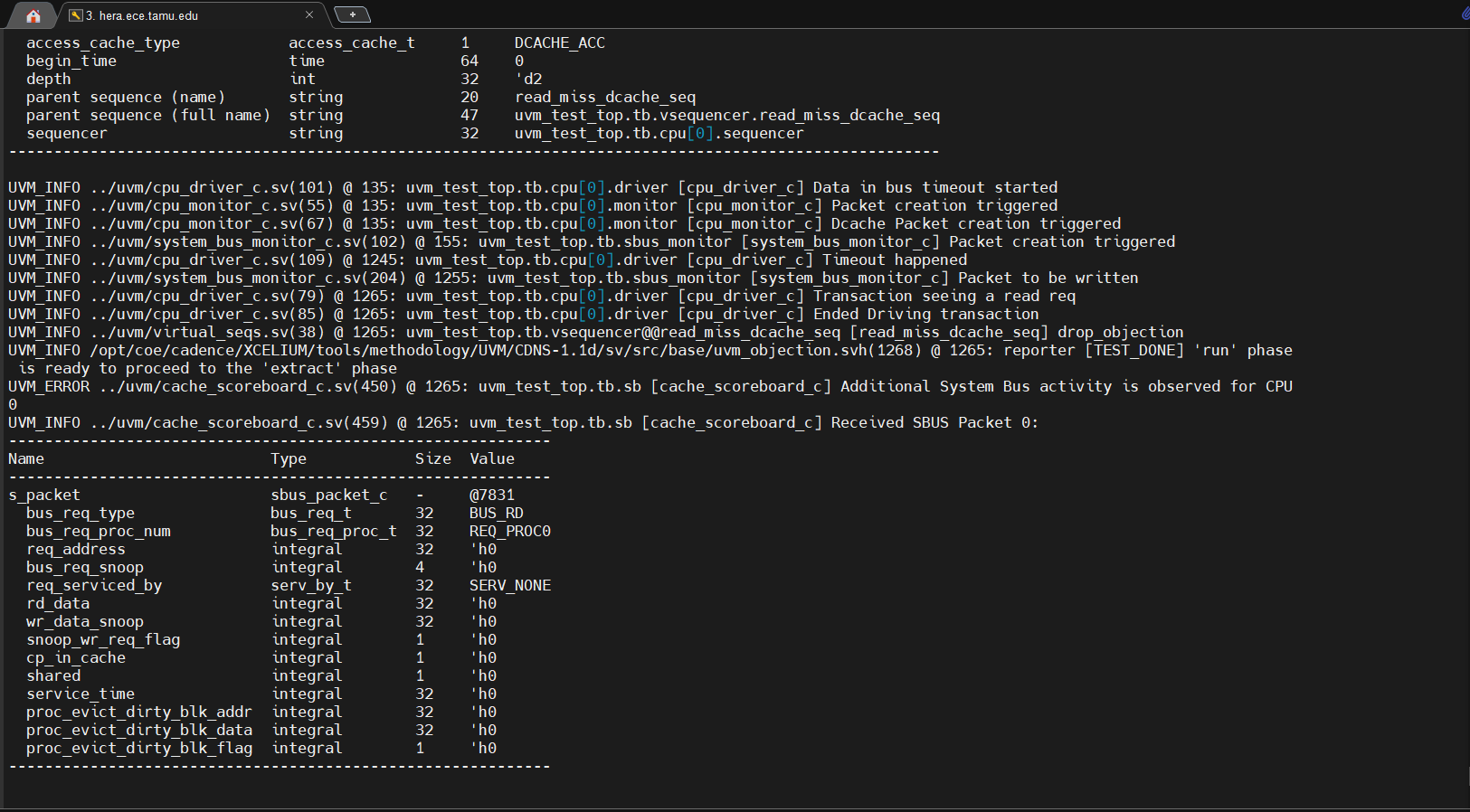
1. **Failing assertion that helped you identify the bug**

This assertion checks for timeout on the read request.

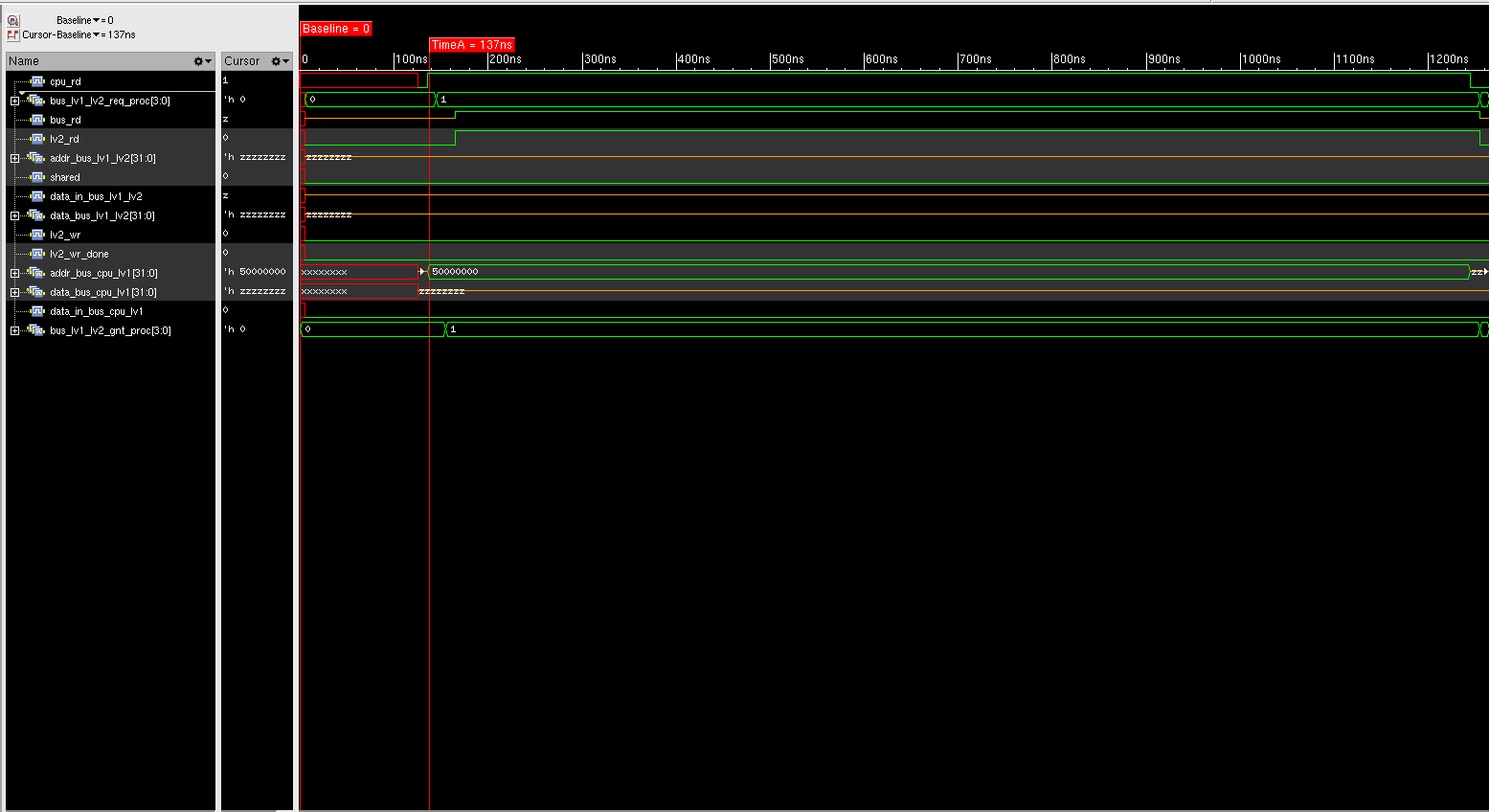
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1. **Debugging:**

Error message:

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Waveform was observed, and it was found that addr\_bus\_lv1\_lv2 was not being asserted. So the design files were checked for address bus assignments.

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1. **Erroneous RTL file name**

main\_func\_lv1\_dl.sv

1. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**

104. assign addr\_bus\_lv1\_lv2 = data\_bus\_lv1\_lv2\_reg;

1. **Corrected RTL code (only mention the corrections)**

104. assign addr\_bus\_lv1\_lv2 = addr\_bus\_lv1\_lv2\_reg;